



[10191/3714]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s) : Klaus RINGGER et al.
Serial No. : 10/520,973
Filed : June 9, 2005
For : PROTECTIVE DEVICE FOR A VEHICLE
Examiner : Tuan C. To
Art Unit : 3663
Confirmation No. : 6449

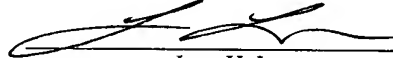
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APPELLANTS' AMENDED APPEAL BRIEF
UNDER 37 C.F.R. § 41.37

S I R :

This Amended Appeal Brief is submitted in response to the PTO communication mailed on July 9, 2007. Applicants filed a Notice of Appeal dated November 27, 2006 (received at the PTO on December 1, 2006), appealing from the Final Office Action dated June 27, 2006, in which claims 11-20 of the above-identified application were finally rejected. This Amended Brief is submitted by Applicants in support of their appeal.

I. REAL PARTY IN INTEREST

The real party in interest in the present appeal is Robert Bosch GmbH of Stuttgart, Germany. Robert Bosch GmbH is the assignee of the entire right, title, and interest in the present application.

II. RELATED APPEALS AND INTERFERENCES

No appeal or interference which will directly affect, or be directly affected by, or have a bearing on, the Board's decision in the pending appeal is known to exist to the undersigned attorney or is believed by the undersigned attorney to be known to exist to Applicants.

III. STATUS OF CLAIMS

Claims 11-20 are pending in the present application, and claims 11-20 are being appealed. Claims 1-10 were canceled in the Preliminary Amendment dated January 11, 2005. Among the appealed claims, claim 11 is independent, and claims 12-20 ultimately depend on claim 11.

IV. STATUS OF AMENDMENTS

No amendment has been made subsequent to the final Office Action mailed on June 27, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

With respect to independent claim 11, the present invention provides a protective device for a vehicle, the protective device including:

a switch (Fig. 1, element 1; Fig. 2, element 19) to deactivate the protective device; (Substitute Specification, p. 4, l. 9-10 & 23-24);

a processor (Figs. 1 and 2, element 9); (p. 4, l. 23-24); and

an additional module (Figs. 1 and 2, element 8) having at least one logic module; (p. 4, l. 15-16 & 18-22);

wherein a switch position is verifiable by the processor (9) and by the additional module (8) independently from one another (p. 4, l. 16-20).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are presented for review on appeal in this case:

(A) Whether pending claims 11-13 and 17-20 are anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 5,513,878 (“Ueda”).

(B) Whether claim 14 is unpatentable under 35 U.S.C. § 103(a) over Ueda in view of U.S. Patent Application Publication No. 2004/0045760 (“Baumgartner”).

(C) Whether claims 15-16 are unpatentable under 35 U.S.C. § 103(a) over Ueda in view of U.S. Patent No. 5,570,903 (“Meister”).

VII. ARGUMENTS

A. Claims 11-13 and 17-20

Claims 11-13 and 17-20 were rejected under 35 U.S.C. § 102(b) as anticipated by United States Patent No. 5,513,878 (“Ueda”). Applicants respectfully submit that the rejection should be withdrawn in view of the following explanation.

To anticipate a claim under § 102(b), a single prior art reference must identically disclose each and every claim element. See Lindeman Maschinenfabrik v. American Hoist and Derrick, 730 F.2d 1452, 1458 (Fed. Cir. 1984). If any claimed element is absent from a prior art reference, it cannot anticipate the claim. See Rowe v. Dror, 112 F.3d 473, 478 (Fed. Cir. 1997). Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claim invention, arranged exactly as in the claim. Lindeman, 703 F.2d 1458 (Emphasis added). Additionally, not only must each of the claim limitations be identically disclosed, an anticipatory reference must also enable a person having ordinary skill in the art to practice the claimed invention, namely the inventions of the rejected claims, as discussed above. See Akzo, N.V. v. U.S.I.T.C.,

1 U.S.P.Q.2d 1241, 1245 (Fed. Cir. 1986). To the extent that the Examiner may be relying on the doctrine of inherent disclosure for the anticipation rejection, the Examiner must provide a “basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flow from the teachings of the applied art.” (See M.P.E.P. § 2112; emphasis in original; see also Ex parte Levy, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)).

Claim 11 recites a protective device for a vehicle, which includes **a switch to deactivate** the protective device, a processor, and an additional module having at least one logic module, wherein **“a switch position is verifiable by the processor and by the additional module independently from one another.”** In support of the rejection of claim 11, the Examiner contends in the Advisory Action (mailed on October 24, 2006) that Ueda teaches the claimed limitation that “a switch position is verifiable by the processor and by the additional module independently from one another.” In an attempt to support this assertion, the Examiner makes the following statements:

[T]he position of the transistor switch (71) is based on the binary signal output of the AND gate (7), said signal generated based on the signal Sc from OR gate (6). The binary Sc signal is generated based on the signal SA from the processor (2A). It is clearly to see a verification can be established by the AND gate, for example a low level signal or a high level signal provided to the switch (71), via the AND gate and the processor (2A).

Regarding the above-noted statements made by the Examiner, Applicants initially note that the contention of the AND gate (7) being equivalent to the claimed “additional module” is made for the first time in the Advisory Action (the Examiner previously contended in the Final Action of 6/27/06 that the OR gate (6) was equivalent to the claimed “additional module”). In any case, Applicants note that the Examiner is clearly misinterpreting the meaning of the claimed feature that **“a switch position is verifiable by the processor and by the additional module independently from one another.”** To the extent the Examiner is contending that “a verification can be established by the AND gate” because “a low level signal or a high level signal [is] provided to the switch (71), via the AND gate and the processor (2A),” the Examiner is contending that merely providing “a low level signal or a high level signal provided to the switch (71), via the AND gate and the processor (2A)” is

equivalent to “verifying” the “switch position,” which assertion is completely flawed both factually and legally: it is a fundamental rule of claim interpretation that the claims should be given “the broadest **reasonable** interpretation” **that is consistent with the specification and the interpretation that those skilled in the art would reach**. (See M.P.E.P. 2111, citing In re Hyatt, 211 F.3d 1367 (Fed. Cir. 2000), and In re Cortright, 165 F.3d 1353 (Fed. Cir. 1999)). The interpretation asserted by the Examiner completely ignores the plain and widely-accepted definition of the term “verify,” which is “to prove the truth of, as by evidence or testimony; confirm; substantiate,” as can be from any dictionary definition, and which plain and widely-accepted definition is entirely consistent with Applicants’ own definition provided in the Specification (see, e.g., page 1, lines 18-21, which indicates that the independent verification involves analyzing the switch position). Accordingly, in order to satisfy the “verify” feature of claim 11, both the processor and another module must each be able to independently analyze the switch position to confirm the switch position. However, there is absolutely no suggestion of any such analysis or confirmation of the switch position in Ueda, as explained further below.

Ueda discloses an electronic system for activating a vehicle rider protection system, which includes three independent processing circuits for processing an acceleration signal to determine whether a collision has taken place or not. In contrast to the claimed feature that “**a switch position is verifiable** by the processor and by the additional module independently from one another,” transistor switch 71 of Ueda is not verifiable independently by the processor and another module, since according to FIG. 2 of Ueda the “OR” gate 6 and “AND” gate 7 merely output signals, and there is no suggestion of any verification or analysis. To the extent the Examiner may be contending that the claimed feature that “**a switch position is verifiable . . .**” is satisfied because it may be theoretically possible for the AND gate (7) to perform a verification (i.e., an analysis or confirmation), there is simply no reasonable basis to contend that an AND gate has an analysis or confirmation capability. In any case, even if it were theoretically possible for the AND gate (7) to perform a verification (with which assumption Applicants do not agree), there is no such suggestion in Ueda, and a mere theoretical possibility of a verification capability cannot support an anticipation conclusion. Furthermore, there is no reasonable basis to contend that the AND gate (7) inherently performs an analysis or confirmation, since there is no “basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flow from the teachings of the applied art.”

Independent of the above, to the extent the Examiner is contending that “a verification can be established by the AND gate” because “a low level signal or a high level signal [is] provided to the switch (71), via the AND gate and the processor (2A),” any theoretical “verification” by the AND gate cannot be independent of the verification by the processor (2A) since the Examiner acknowledges that the position of the transistor switch (71) is ultimately dependent on the signal SA from the processor (2A).

Independent of the above, in contrast to the claimed feature of a “switch to deactivate the protective device,” as recited in claim 11, the transistor switch (71) of Ueda provides an ignition current activating the ignition element and consequently a triggering of the airbag, which is completely opposite of the claimed feature. Clearly, transistor 71 is not a switch to deactivate the protective device since the transistor 71 is made conductive if a collision occurs, i.e., the transistor 71 cannot, and should not, be used to deactivate the protective device since its activation is used to indicate the occurrence a collision.

Accordingly, for at least these reasons, it is respectfully submitted that Ueda does not anticipate claim 11. With respect to claims 12, 13 and 17-20, which ultimately depend from claim 11 and therefore include all of the limitations of claim 11, it is respectfully submitted that Ueda does not anticipate these dependent claims for at least the same reasons given above in support of the patentability of claim 11. Reversal of this anticipation rejection is therefore respectfully requested.

B. Claim 14

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ueda in view of U.S. Patent Application Publication No. 2004/0045760 (“Baumgartner”).

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438

(Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

Applicants note that claim 14 ultimately depends on claim 11. Even if it were proper to combine the applied references as suggested by the Examiner (which is not conceded), the secondary Baumgartner reference does not cure the critical deficiencies of the Ueda reference (as explained above) with respect to base claim 11. Indeed, the Office Action merely uses Baumgartner for the alleged disclosure of a time response modification. Accordingly, claim 14 is patentable for the above reasons and the reasons given in support of the patentability of parent claim 11. Therefore, reversal of the obviousness rejection is requested.

C. Claims 15-16

Claims 15 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ueda in view of U.S. Patent No. 5,570,903 (“Meister”).

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

Applicants note that claims 15 and 16 ultimately depend on claim 11. Even if it were proper to combine the references as suggested by the Examiner (which is not conceded), the secondary Meister reference does not cure the critical deficiencies of the Ueda reference (as explained above) with respect to base claim 11. Indeed, the Office Action

merely uses Meister for the alleged disclosure of a resistor network and a Hall-effect sensor. Accordingly, claims 15 and 16 are patentable for the above reasons and the reasons given in support of the patentability of parent claim 11. Therefore, reversal of the obviousness rejection is requested.

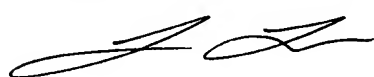
VIII. CONCLUSION

For the foregoing reasons, it is respectfully submitted that the final rejections of claims 11-20 should be reversed.

Claims Appendix, Evidence Appendix and Related Proceedings Appendix sections are found in the attached pages.

Respectfully submitted,

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APPENDIX TO APPELLANTS' APPEAL BRIEF
UNDER 37 C.F.R. § 41.37

CLAIMS APPENDIX

The claims involved in this appeal, claims 11-20, in their current form after entry of all amendments presented during the course of prosecution, are set forth below:

11. A protective device for a vehicle, comprising:
 - a switch to deactivate the protective device;
 - a processor; and
 - an additional module having at least one logic module,wherein a switch position is verifiable by the processor and by the additional module independently from one another.
12. The protective device of claim 11, wherein the at least one logic module includes at least one of a gate and a flip-flop.
13. The protective device of claim 11, wherein the logic module is configured so that a time response of a logic state of the logic module is modifiable.
14. The protective device of claim 13, wherein the processor modifies the time response.
15. The protective device of claim 11, wherein the switch includes a resistor network.
16. The protective device of claim 11, wherein the switch includes at least one Hall-effect sensor.
17. The protective device of claim 11, further comprising:
 - a control unit to power the switch.
18. The protective device of claim 11, wherein the switch is powered from an external supply.
19. The protective device of claim 11, wherein the logic state of the logic module is allowed to be retained.
20. The protective device of claim 11, further comprising:
 - a triggering circuit control; and

an AND gate connectible to the triggering circuit control, wherein the module and the processor are connected to the AND gate.

EVIDENCE APPENDIX

In the present application, there has been no evidence submitted pursuant to 37 C.F.R. §§ 1.130, 1.131 or 1.132, or other evidence entered by the Examiner and relied upon by Appellants in the present appeal.

RELATED PROCEEDINGS APPENDIX

No appeal or interference which will directly affect, or be directly affected by, or have a bearing on, the Board's decision in the pending appeal is known to exist.